

PTO/SB/08A (Substitute for form 1449/PTO)	Attorney Docket No.: 023-0030
	Application No.: 10/729,844
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: En-Hsing Chen
	Filing Date: December 5, 2003
	Group Art Unit: 2827
	Examiner Name: Mai, Son Luu
Sheet 1 of 1	Date Submitted: June 29, 2005

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional).

²See Kinds Codes of USPTO Patent Documents at www.uspto.gov/ or MPEP 901.04.

³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3)

⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.

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		Examiner Name: Son Luu Mai
Sheet 1 of 2		Date Submitted: April 18, 2005

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JM	AA	DURISETY, CHANDRA SEKHAR ACHARYULU, "Analysis and Characterization of Single-Poly Floating Gate Devices in 0.35um PDSOI Process", A Thesis Presented for the Master of Science Degree, The University of Tennessee, Knoxville, December 2002, pp. i-viii and 1-80.	/
JM	AB	EVANS, ROBERT J., ET AL., "Energy Consumption Modeling and Optimization for SRAM's," IEEE Journal of Solid-State Circuits, Vol. 30, No. 5, May 1995, pp. 571-579.	/
JM	AC	JUNG, TAE-SUNG, ET AL., "A 117-mm ² 3.3-V Only 128-Mb Multilevel NAND Flash Memory for Mass Storage Applications," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1575-1583.	/
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JM	AF	KIM, BYUNGCHUL, ET AL., "A Scaled SONOS Single-Transistor Memory Cell for a High-Density NOR Structure with Common Source Lines," Journal of the Korean Physical Society, Vol. 41, No. 6, December 2002, pp. 945-948.	/
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JM	AI	LEE, YONG KYU, ET AL., "Multilevel Vertical-Channel SONOS Nonvolatile Memory on SOI," IEEE Electron Device Letters, Vol. 23, No. 11, November 2002, pp. 664-666.	/
JM	AJ	LIN, HORNG-CHIH, ET AL., "Ambipolar Schottky-Barrier TFTs," IEEE Transactions on Electron Devices, Vol. 49, No. 2, February 2002, pp. 264-270.	/
JM	AK	NAJEEB-UD-DIN ET AL., "Analysis of Floating Body Effects in Thin Film Conventional and Single Pocket SOI MOSFETs Using the GIDL Current Technique", IEEE Electron Device Letters, Vol. 23, No. 4, April 2002, pp. 209-211.	/
JM	AL	NISHIHARA, TOSHIYUKI, ET AL., "A Quasi-Matrix Ferroelectric Memory for Future Silicon Storage," IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp. 1479-1484.	/
JM	AM	PARK, KI-TAE, "Recent Non-Volatile Memory Device & Circuit Technology," Halo LSI Inc, (date unknown), 35 pages.	/
JM	AN	ROIZIN, YAKOV, ET AL., "Plasma-Induced Charging in Two Bit per Cell SONOS Memories," Tower Semiconductor Ltd., Migdal HaEmek 23105, Israel, (date unknown), 4 pages.	/
Examiner Signature		son mm	Date Considered
			07/08/05

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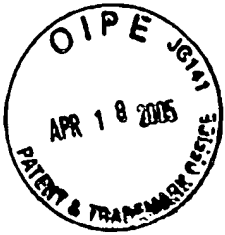
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	Examiner Name: Son Luu Mai
Sheet 2 of 2	Date Submitted: April 18, 2005

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Examiner Initials*	Cite No. ¹	Include name of author (In CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JM	AO	SHIN, JONGSHIN, ET AL., "A New Charge Pump Without Degradation in Threshold Voltage Due to Body Effect," IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000, pp. 1227-1230.	✓
JM	AP	STURM, J. C., ET AL., "Leakage Current Modeling of Series-Connected Thin Film Transistors," IEEE Transactions on Electron Devices, Vol. 42, No. 8, August 1995, pp. 1561-1563.	✓
JM	AQ	SUGIBAYASHI, TADAHICO, ET AL., "A 30-ns 256-Mb DRAM with a Multidivided Array Structure," IEEE Journal of Solid-State Circuits, Vol. 28, No. 11, November 1993, pp. 1092-1098.	✓
JM	AR	SUH, KANG-DEOG, ET AL., "A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme," IEEE Journal of Solid-State Circuits, Vol. 30, No. 11, November 1995, pp. 1149-1156.	✓
JM	AS	TAKEUCHI, KEN, ET AL., "A Negative V _{th} Cell Architecture for Highly Scalable, Excellently Noise-Immune, and Highly Reliable NAND Flash Memories," IEEE Journal of Solid-State Circuits, Vol. 34, No. 5, May 1999, pp. 675-684.	✓
JM	AT	THEAN, AARON, ET AL., "Flash memory: towards single-electronics," IEEE Potentials, October/November 2002, pp. 35-41.	
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	BD		
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LIST OF PENDING U. S. PATENT APPLICATIONS

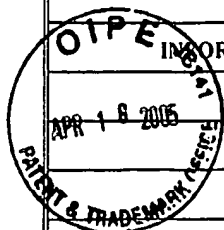
The following pending U.S. patent applications are listed for consideration by the Examiner.

- jk
- 1) U.S. Patent Application No. 10,729,865, filed December 5, 2003, entitled "NAND Memory Array Incorporating Multiple Series Selection Devices and Method for Operation of Same," naming inventors En-Hsing Chen, Andrew J. Walker, Roy E. Scheuerlein, Sucheta Nallamothe, Alper Ilkbahar, Luca G. Fasoli and James M. Cleaves.
 - jk 2) U.S. Patent Application No. 10/729,843, filed December 5, 2003, entitled "Memory Array Incorporating Memory Cells Arranged in NAND Strings," naming inventors Luca G. Fasoli, Roy E. Scheuerlein, En-Hsing Chen, Sucheta Nallamothe, Maitreyee Mahajani, and Andrew J. Walker.

<u>EXAMINER</u>	<u>DATE CONSIDERED</u>
SON MAI	07/08/05

Applicant(s) are providing a separate list of pending applications, pursuant to MPEP § 609III(D), to avoid publication of the application numbers on any patent that issues from the above-identified application. Applicant(s) request that the Examiner indicate consideration of the pending applications listed above in accordance with MPEP 609III(C)(2) and return a copy of this page with the next communication.

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U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
AL	AA	4,142,176	02-27-1979	Dozier		
PM	AB	4,543,594	09-24-1985	Mohsen et al.		
PM	AC	4,602,354	07-22-1986	Craycraft et al.		
PM	AD	4,868,616	09-19-1989	Johnson et al.		
PM	AE	5,197,027	03-23-1993	Challa		
PM	AF	5,301,144	04-05-1994	Kohno		
PM	AG	5,412,493	05-02-1995	Kunii et al.		
PM	AH	5,429,968	07-04-1995	Koyama		
PM	AI	5,473,563	12-05-1995	Suh et al.		
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PM	AK	5,621,683	04-15-1997	Young		
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PM	AM	5,703,382	12-30-1997	Hack et al.		
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PM	AN	JA 62-142363	06-25-1987			
PM	AO	JA 62-155568	07-10-1987			
PM	AP	JA-2001-358237	12-26-2001			
PM	AQ	JA-2002-280467	09-27-2002			
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SM	AR	5,715,194	02-03-1998	Hu	
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SM	AT	5,814,853	09-29-1998	Chen	
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	BE					
	BF					
	BG					
	BH					
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FM	BZ	6,515,888	02-04-2003	Johnson et al.	
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PM	CH	6,822,903 B2	11-23-2004	Scheuerlein et al.	
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PM	CJ	6,856,572 B2	02-15-2005	Scheuerlein et al.	
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PM	CL	US RE. 35,838	07-07-1998	Momodomi et al.	

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	CO					
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JM	CQ	US-2002/0021587 A1.	02-21-2002	Sakui et al.	
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JM	CT	US-2004/0124415	07-01-2004	Walker et al.	
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JM	CX	US-6,108,238	08-2000	Nakamura et al.	
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JM	DA	US-5,812,457	09-1998	Arase	
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	DC				

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